TSMC-02-1314

April 30, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/822,193 04/30/04

Chien-Jung Wang

A NOVEL TEST STRUCTURE FOR SPEEDING A STRESS-INDUCED VOIDING TEST AND METHOD OF USING SAME

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on May 4, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date Stephen B. Ackerman 5/4/04

U.S. Patent 6,037,795 to Filippi et al., "Multiple Device Test Layout," describes a multiple device test layout.

U.S. Patent 6,191,481 to Bothra et al., "Electromigration Impeding Composite Metallization Lines and Methods for Making the Same," describes electromigration impeding composite metallization lines and methods for making the same.

U.S. Patent 5,973,402 to Shinriki et al., "Metal Interconnection and Method for Making," describes a metal interconnection and a metod for making the same.

U.S. Patent 5,504,017 to Yue et al., "Void Detection in Metallization Patterns," describes void detection in metallization patterns.

U.S. Patent 5,156,909 to Henager, Jr. et al., "Thick, Low-Stress Films, and Coated Substrates Formed Therefrom, and Methods for Making Same," describes thick, low-stress films, and coated substrates formed therefrom, and methods for making same.

U.S. Patent 5,010,024 to Allen et al., "Passivation for Integrated Circuit Structures," describes passivation for integrated circuit structures.

The following two U.S. Patents describe a method of reducing incidence of stress-induced voiding in semiconductor interconnect lines:

1) U.S. Patent 6,174,743 to Pangrle et al., "Method of Reducing Incidence of Stress-Induced Voiding in Semiconductor Interconnect Lines."

2) U.S. Patent 6,221,794 to Pangrle et al., "Method of Reducing Incidence of Stress-Induced Voiding in Semiconductor Interconnect Lines."

U.S. Patent 5,550,405 to Cheung et al., "Processing Techniques for Achieving Production-Worthy, Low Dielectric, Low Interconnect Resistance and High Performance ICs," discusses semiconductor devices having a reduced RC (resistance times capacitance) time constant and hence faster speed.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

TSMC-02-1314

April 30, 2004

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/822,193 04/30/04

Chien-Jung Wang

A NOVEL TEST STRUCTURE FOR SPEEDING A STRESS-INDUCED VOIDING TEST AND METHOD OF USING SAME

ASSOCIATE POWER OF ATTORNEY

I hereby appoint Stephen G. Stanton, registration number 35,690, as my associate attorney in this case. His telephone number is (610) 296-5194.

Please continue to direct all correspondence in this case to the undersigned attorney.

Respectfully submitted,

Stephen B. Ackerman,

Principal attorney of record

Sheet 1 of 1

Form PTO-1449 MAY 0 6 2004 JC24

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
TSMC-02-1314	10/822,193
Applicant: Chien-Jung Wang	
Filing Date: 04/09/04	Group Art Unit:

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6037795	3/14/00	Filippi et al.	324	763	9/26/97
	6191481	2/20/01	Bothra et al.	257	734	12/18/98
	5973402	10/26/99	Shinriki et al.	257	768	1/30/97
	5504017	4/2/96	Yue et al.	437	8	12/20/94
	5156909	10/20/92	Henager, Jr. et al.	428	334	11/28/89
	6174743	1/16/01	Pangrle et al.	438	14	12/8/98
	6221794	4/24/01	Pangrle et al.	438	792	12/8/98
	5550405	8/27/96	Cheung et al.	257	642	12/21/94
	5010024	4/23/91	Allen et al.	437	24	5/15/89

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.